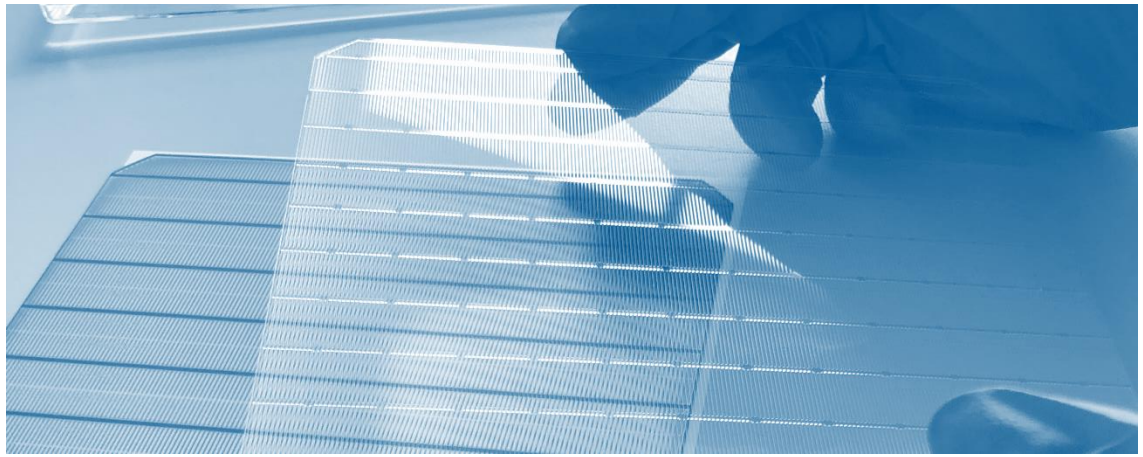

PECVD Interfacial Oxide/*n*-Poly Si Stacks for POLO-IBC Solar Cells

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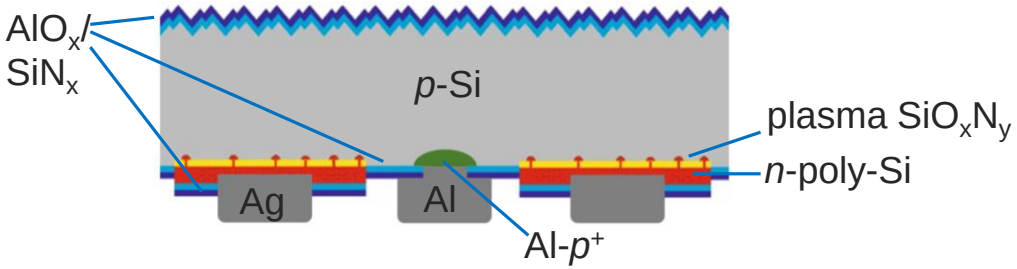
[1]Institute for Solar Energy Research Hamelin (ISFH), Germany

[2]Leibniz Universität Hannover, Germany

[3]LPKF Laser & Electronics AG, Germany

[4]centrotherm international AG, Germany

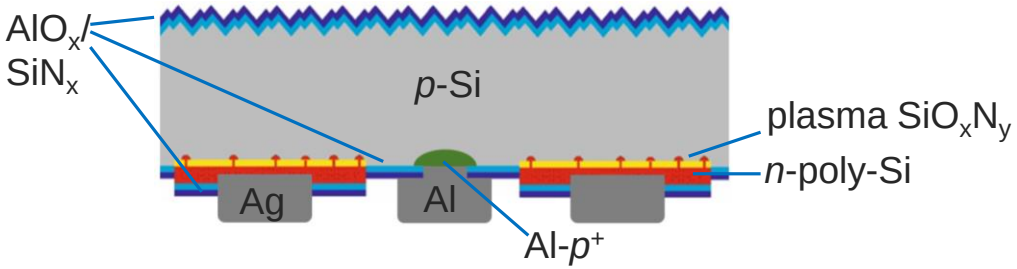
Motivation and overview

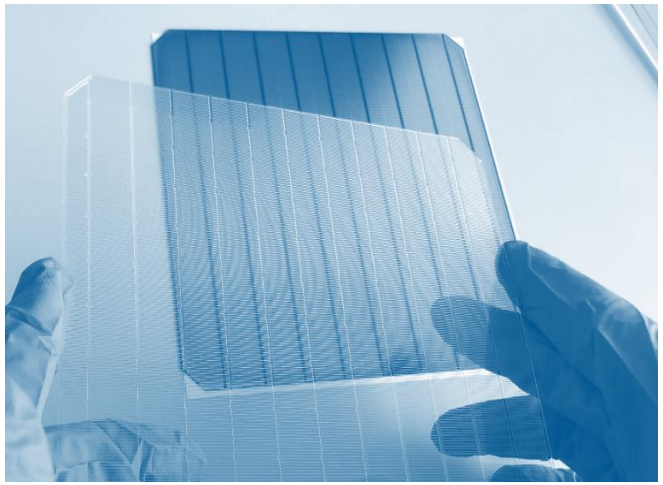


- POLO IBC: implementation of poly-silicon on in a solar cell structure with high reuse of PERC processing steps*1,2
- High simulated efficiency potential of 25.5%*3

*1: EE. Bende et al., 7th Metallization and Interconnection Workshop, Konstanz, Germany (2017).
*2: F. Haase et al., Proc. of the 46th IEEE PVSC, Chicago, IL, USA, 2200-2206 (2019).
*3: C. N. Kruse et al., Scientific Reports, 11, 999 (2021).
*4: M. Stöhr, 37th EUPVSEC, 521 (2020).
*5: T. Dullweber, SNEC (2021).

Motivation and overview





- POLO IBC: implementation of poly-silicon on in a solar cell structure with high reuse of PERC processing steps[*1,2]
- High simulated efficiency potential of 25.5%[*3]
- Our process approach[*4]:
  Local deposition of PECVD-SiO_xN_y/ *n*-a-Si through a glass shadow mask from LPKF laser & Electronics
- Current status (244.32 cm^2): 23.7% (fabrication calibration by ISE CalLab)

[*1]: EE. Bende et al., 7th Metallization and Interconnection Workshop, Konstanz, Germany (2017).
[*2]: F. Haase et al., Proc. of the 46th IEEE PVSC, Chicago, IL, USA, 2200-2206 (2019).
[*3]: C. N. Kruse et al., Scientific Reports, 11, 999 (2021).
[*4]: M. Stöhr, 37th EUPVSEC, 521 (2020).
[*5]: T. Dullweber, SNEC (2021).

POLO IBC process flow

- Texture
- Rear side polish+clean
- PECVD SiO_xN_y + *n*-a-Si
- *n*-poly Si anneal in N_2 atm.
- Front side AlO_x/SiN_x
- Rear side AlO_x/SiN_x
- LCO AlO_x/SiN_x regions
- Screen print Ag/ n-poly regions
- Screen print Al/ AlO_x/SiN_x regions
- Fast firing

PECVD SiO_xN_y and *n*-a Si:

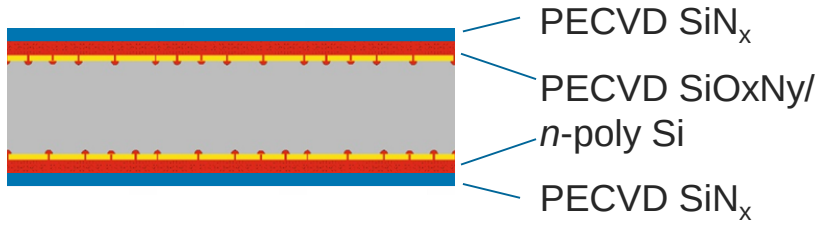
c.plasma tool from centrotherm

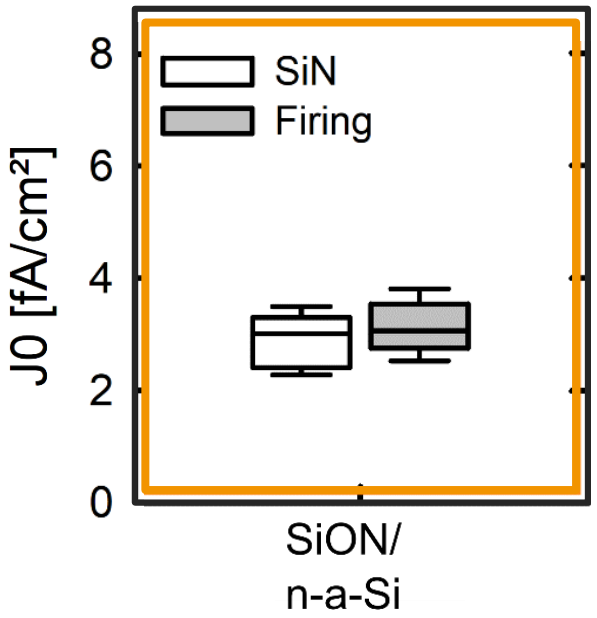
Process step from PERC+

New process step

PECVD *n*-poly Si

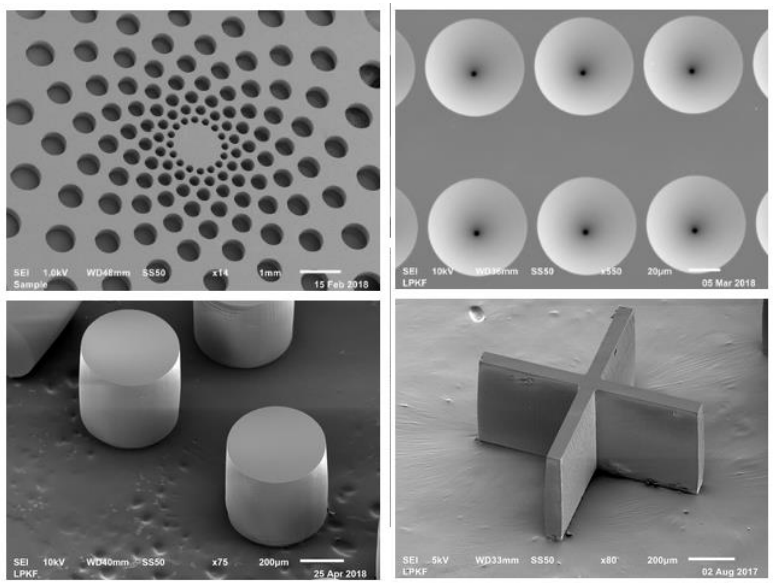
- One-sided deposition technique→ suitable for various cell concepts like Topcon, IBC, …
- Excellent surface passivation after firing step[*1]
- Option to use in-situ grown PECVD SiO_xN_y from N_2O plasma
- Structured deposition through glass shadow mask possible → IBC cell application



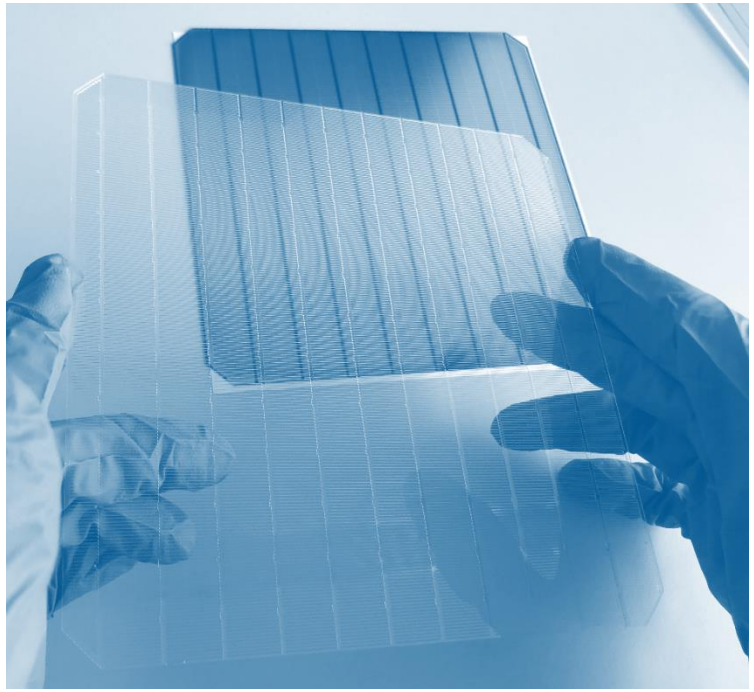


[*1]M. Stöhr et al., ACS Appl. Energy Mater., 4 (5), 4646–4653 (2021)

Shadow masks for local PECVD SiO_xN_y / n-a-Si fingers



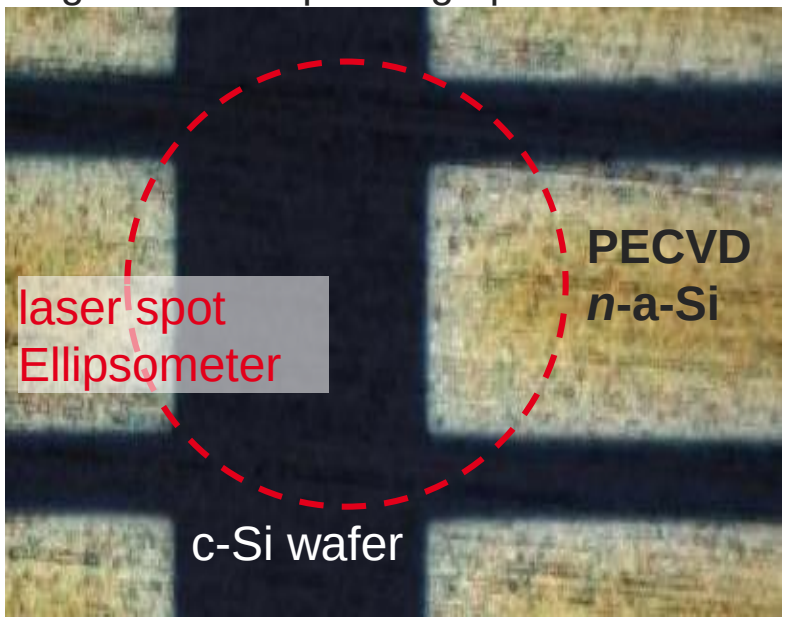
IBC shadow masks



- LPKF Laser & Electronics AG manufactures glass shadow masks with their proprietary Laser-Induced Deep Etching (LIDE) technology for glass structuring
- optimization of shadow mask design for IBC process by ISFH and LPKF

PECVD deposition through glass shadow masks

Light microscope image post PECVD



- Glass mask reduces deposition rate for *n*-a-Si to ~60% compared to full area
- increased deposition time with glass mask not significant for total process time
- Reduced layer thickness also for PECVD SiO_xN_y

adjust oxide thickness experimentally, no easy to apply measurement techniques available

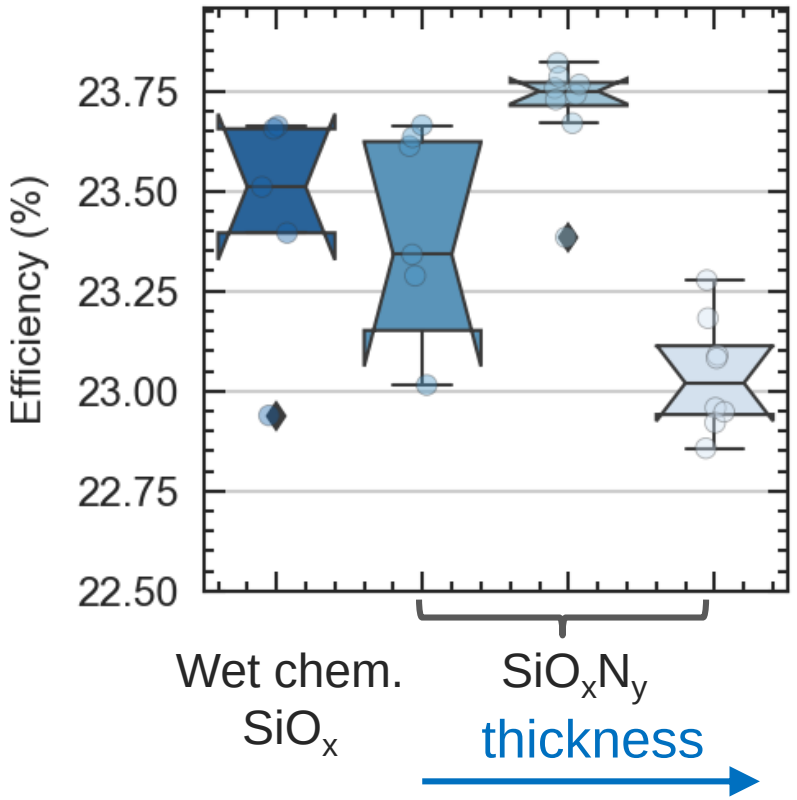
SiO_xN_y experiment

- Variation of interfacial oxide thickness for PECVD SiO_xN_y for optimum contact passivation and current transport

Process optimization on POLO IBC solar cells

A1	A2	A3	A4
Wet. chem. SiO_x	SiO_xN_y		
~1.7 nm	«thin»	«medium»	«thick»
PECVD n-poly Si, ~150 nm			
Polysilicon anneal in N_2 atm.:			
850°C			

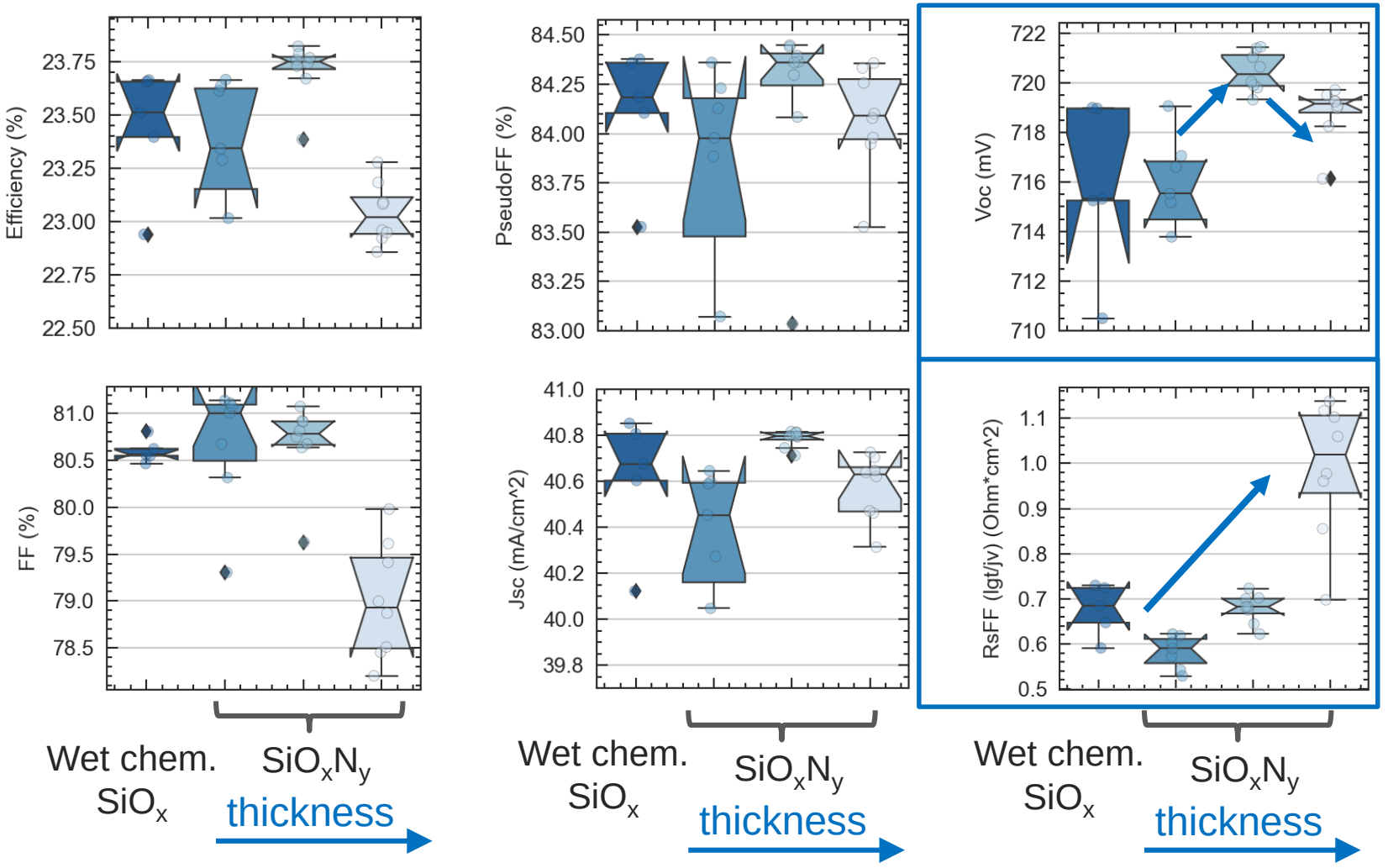
SiO_xN_y thickness variation



Reference with wet chem. SiO_x interface at 23.5% median efficiency

SiO_xN_y: significant impact of oxide thickness on efficiency ranging from 23.0% to 23.75%

SiO_xN_y experiment in detail



- Voc goes through an optimum with increasing oxide thickness
- Fill factor shows decrease with increasing oxide thickness

→ root cause is Rs

„medium" SiO_xN_y thickness gives optimum for passivation and current transport

SiO_x experiment

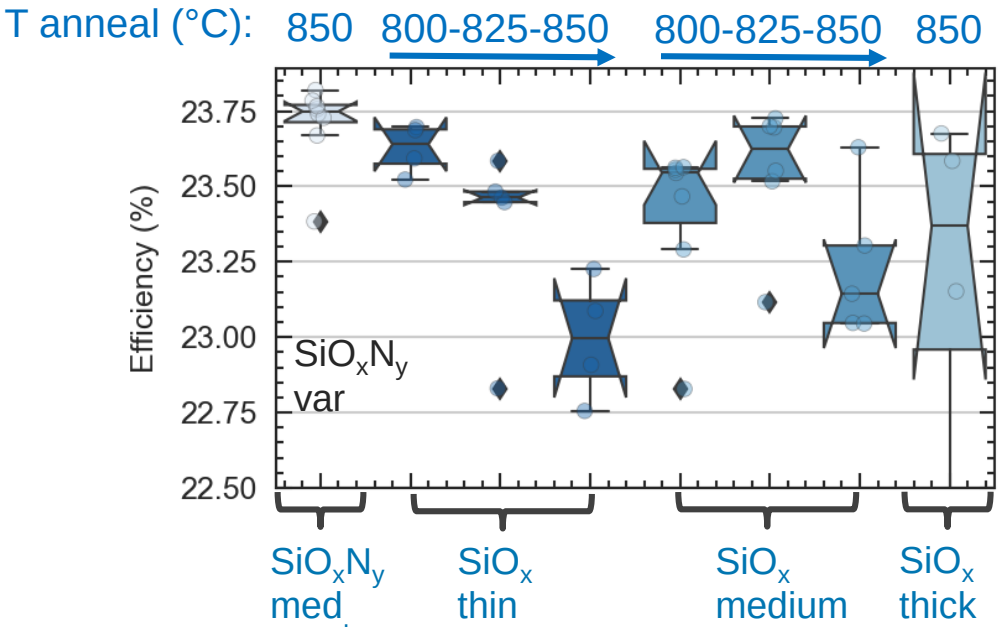
- Investigate O_2 plasma oxidation (PECVD SiO_x) as environmental friendly alternative to N_2O

  Achieves SiO_x similar passivation quality and transport properties as SiO_xN_y?

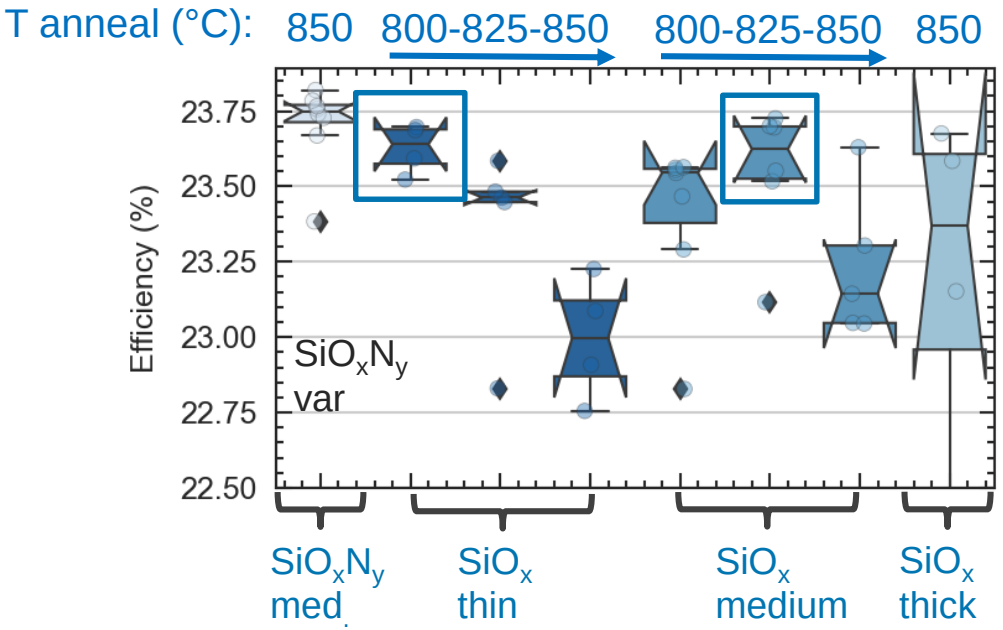
- Compare solar cell optimization by PECVD SiO_x thickness to variation of *n*-poly Si anneal temperature

A3	B1	B2	B3	B4	B5	B6	B7
SiO_xN_y	SiO_x			SiO_x			SiO_x
«med»	«thin»			«medium»			«thick»
PECVD n-poly Si, ~150 nm							
Polysilicon anneal in N_2 atm.:							
850°C	800°C	825°C	850°C	800°C	825°C	850°C	850°C

PECVD SiO_x: var of thickness and *n*-poly anneal Temp.

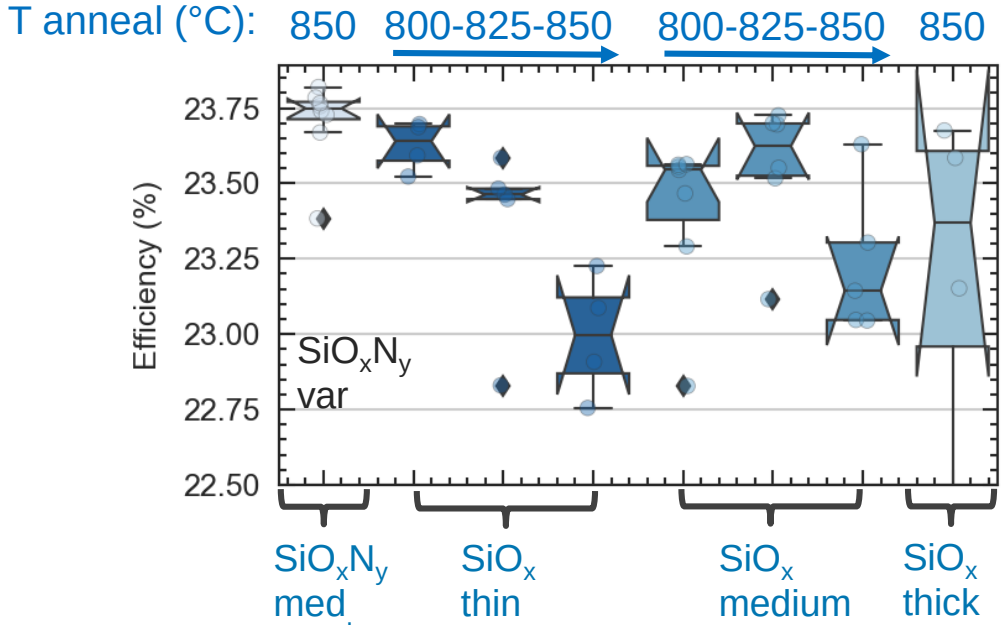


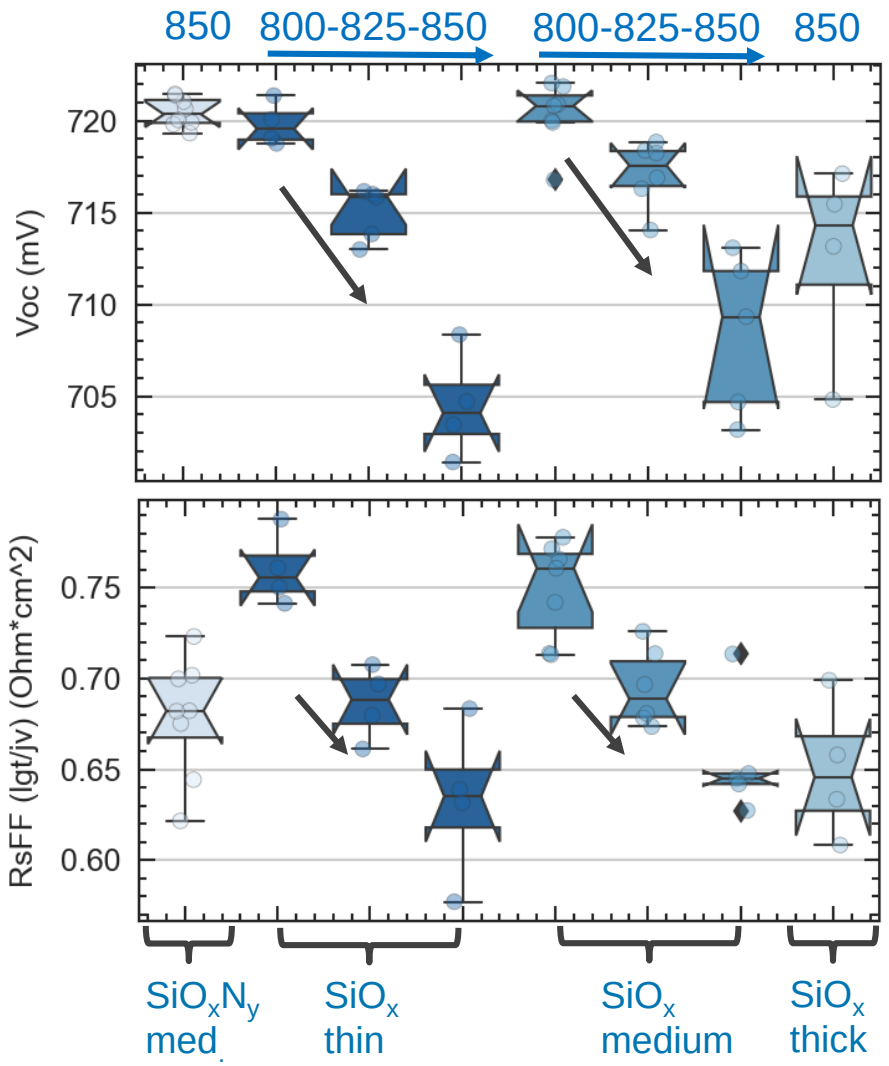
PECVD SiO_x: var of thickness and *n*-poly anneal Temp.



- SiO_x: optimum conditions lead to 23.6% efficiency, close to SiO_xN_y
- Optimum anneal temperature increases for thicker SiO_x from 800°C to 825°C

PECVD SiO_x: var of thickness and *n*-poly anneal Temp.

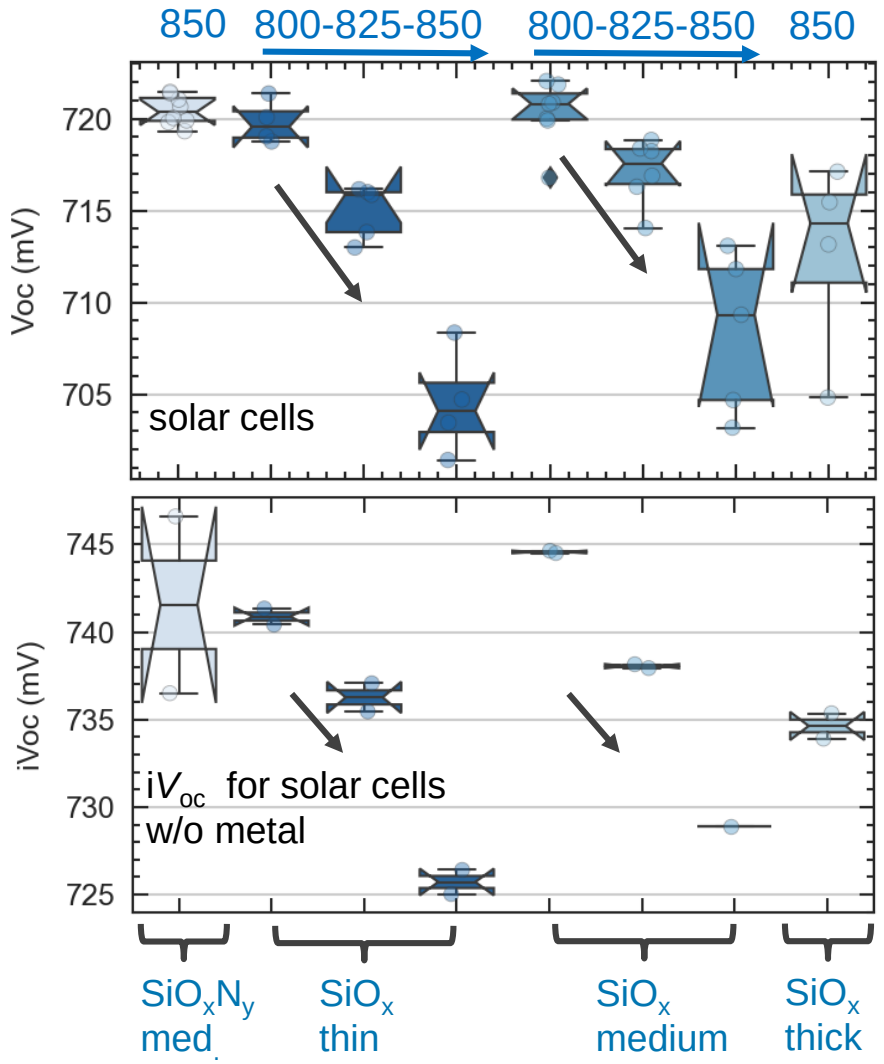




- SiO_x break-up with increasing anneal T leads to decreasing V_{oc} but also improved R_s

PECVD SiO_x: „implied Voc samples“ and full solar cells

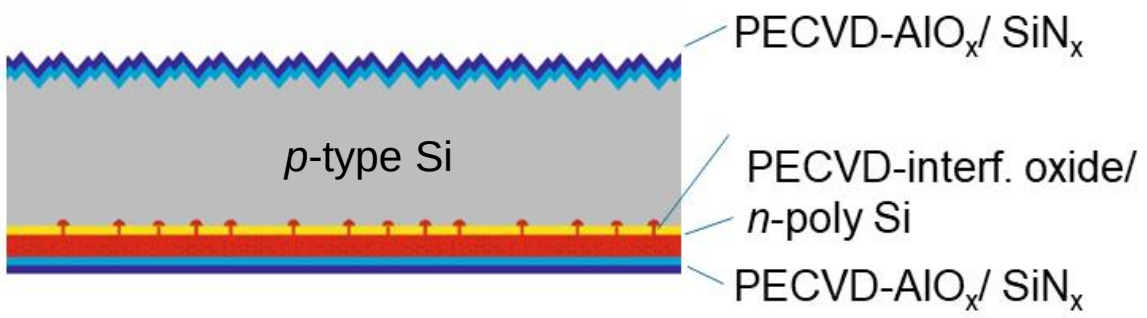
- Same trend for V_{oc} data from full solar cells and iVoc data for solar cells w/o metallization
- Support of oxide break up effect as root cause for V_{oc} loss with increasing anneal T
- Difference between iVoc and Voc ~20 mV due to LCO contacts
- Optimization by LCO layout adjustments, Al paste



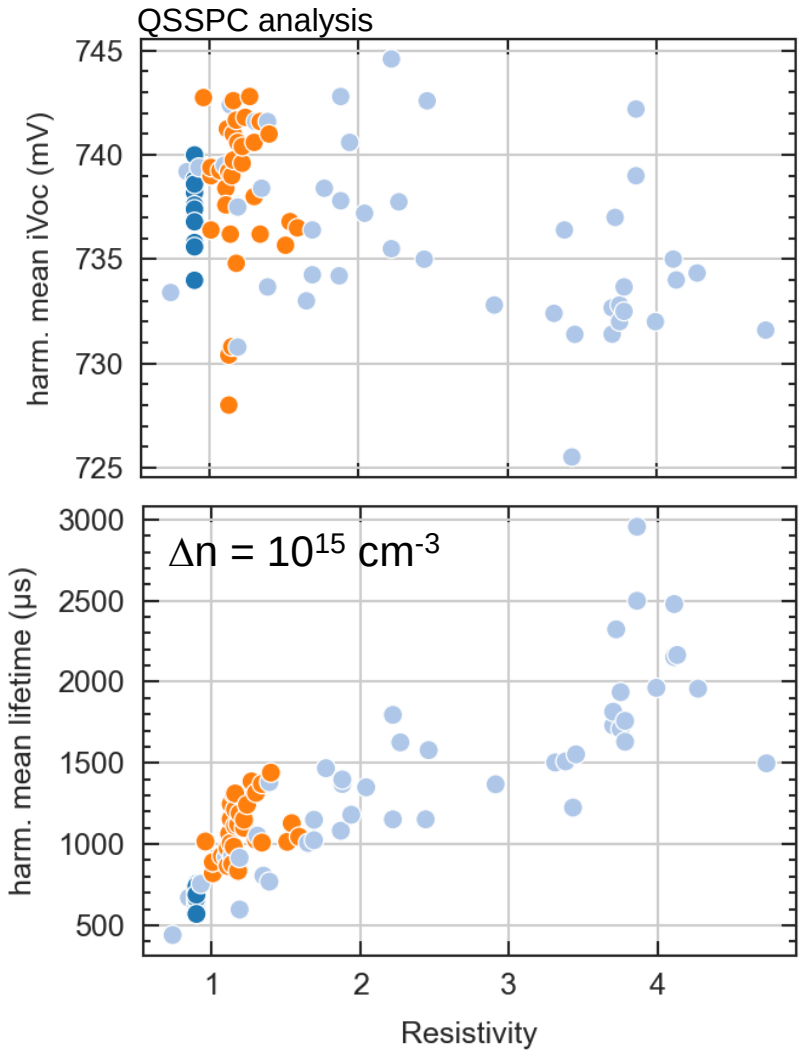
Investigation on p-type Silicon material

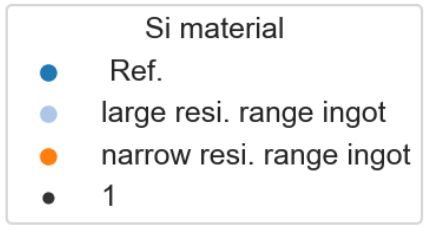
Material specifications

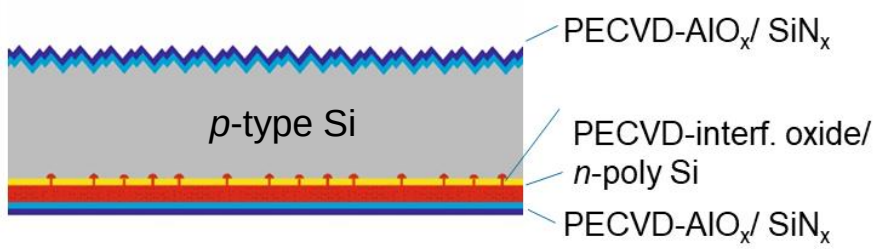
- *p*-type material, Ga-doped
- Resistivity range: 0.7 Ohm*cm – 5 Ohm*cm
- Wafer thicknesses: ~150 µm
- Lifetime test with a POLO IBC like test structure:
  - front side textured, rear side polished
  - rear passivation stack: *n*-type poly-Si/ AlO_x/SiN_x
  - front side passivation: AlO_x/SiN_x



Resistivity dependant lifetime characterization for two p-type Si ingots

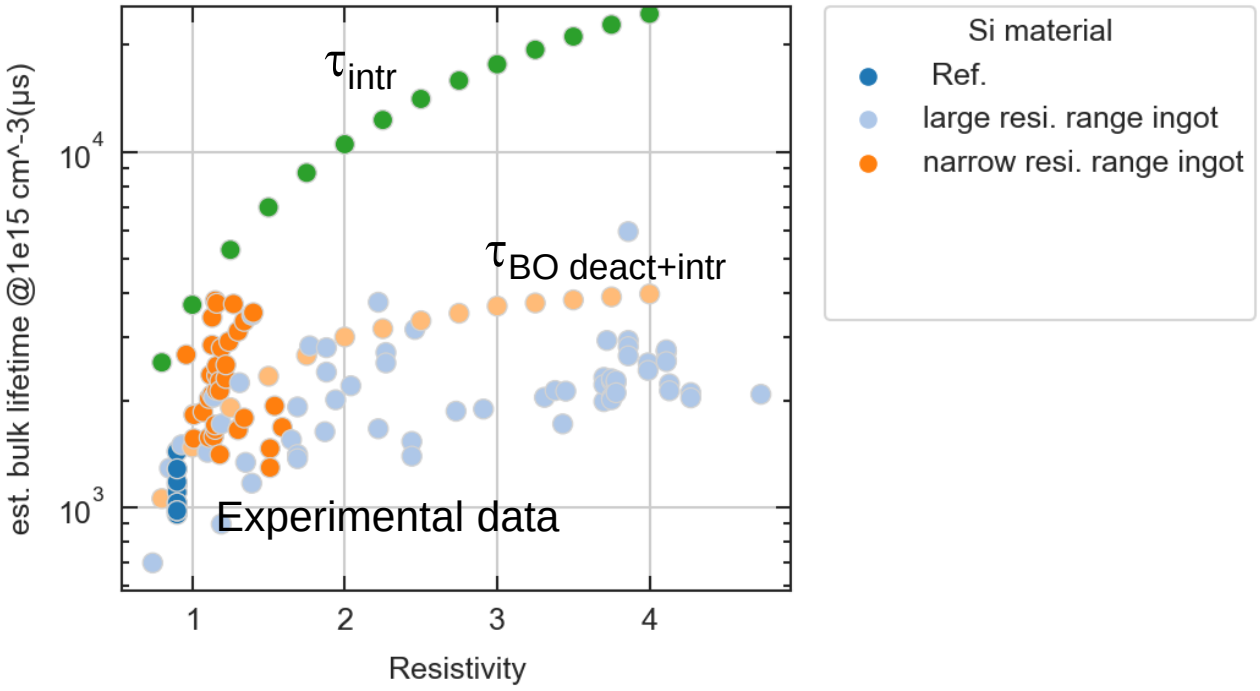






Implied V_{oc} level around 735 mV or better over the resistiviy range investigated

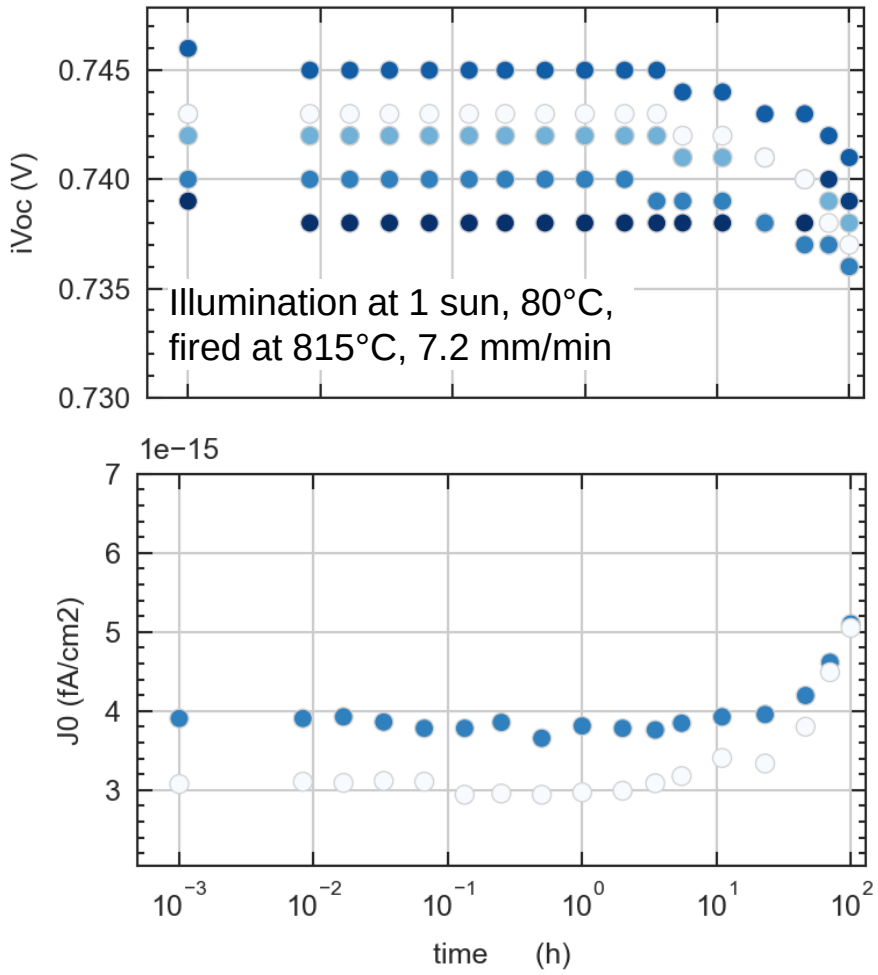
Estimated bulk lifetimes for p-type Si material investigated

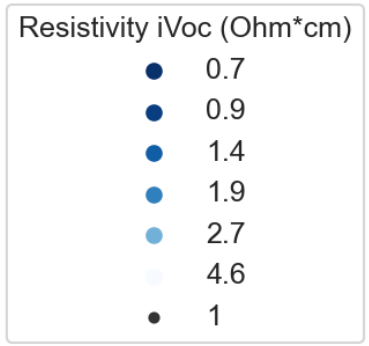


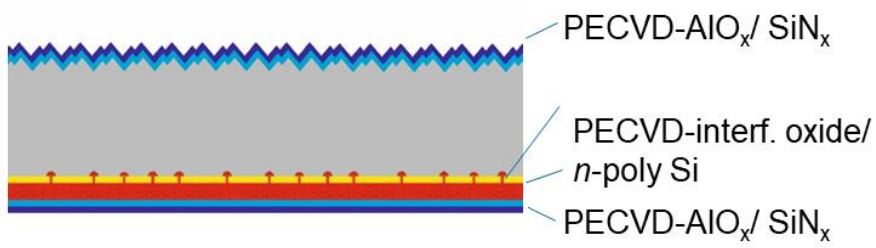
- Calculation of bulk lifetime with $J_{0,\ surfaces} = 8\ fA/cm^2$
- Limits: intrinsic lifetime and BO defect deactivated + intr.
- Experimental bulk lifetimes:
  - in the range of BO deact.+intr. lifetime
  - Low resi range partly significantly better

A. Richter et al., Phys. Rev. B 86, 165202 (2012).
D. Walter et al., Prog. Photovolt. 24, 920 (2016).

Light and elevated temperature tests







- LeTID test for different resistivities of silicon wafer material
- Stable implied Voc values up to 10h, then
- degradation in $J_{0,\,surface}$ leads to decreasing iV_{oc}

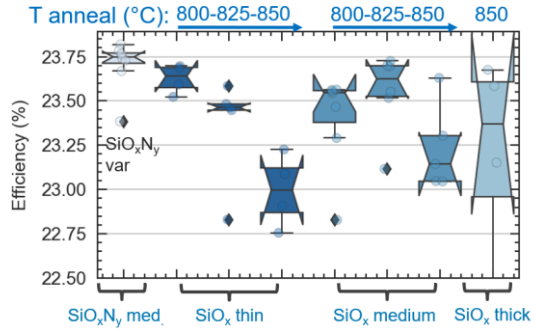
→Further investigations ongoing

Summary

- PECVD-n-poly-Si

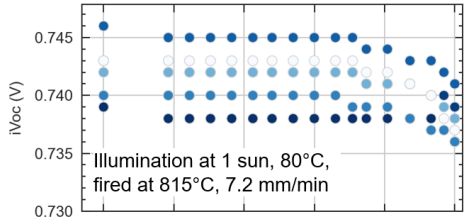
  In-situ PECVD SiO_xN_y and SiO_x allow fine tuning by thickness variation similar to poly Si anneal temperature or thermal SiO_2

  PECVD SiO_xN_y and SiO_x show so far similar efficiencies



- POLO-IBC solar cells:

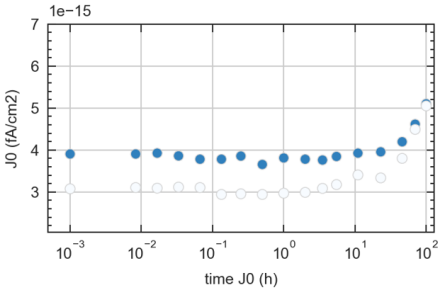
  efficiencies of 23.7%, implied Voc values around 742 mV for cells w/o metal



- Characterization of p-type silicon material from 0.7 to 4 Ohm*cm:

  iVoc around 735 mV in resistivity range for POLO-IBC like test structures

  So far, no significant LETID degradation detected, $J_{0,\,surface}$ degradation under investigation



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- **Thank you for your attention !**

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Federal Ministry for Economic Affairs and Climate Action

on the basis of a decision by the German Bundestag

IBC4EU

State of Lower Saxony, Gemany